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| **COMPUTER ORGANIZATION AND ARCHITECTURE**  **[ Revised Credit System ]**  **(Effective from the academic year 2018-19)**  **SEMESTER - III** | | | |
| **Subject Code** | **CSE 2151** | **IA Marks** | **50** |
| **Number of Lecture Hours/Week** | **04** | **Exam Marks** | **50** |
| **Total Number of Lecture Hours** | **48** | **Exam Hours** | **03** |
| **CREDITS - 04** | | | |
| **Course objectives:** This course will enable students to   * Summarize the fundamental concepts of the organization and architecture of a computer. * Analyze taxonomy of Execution, Processor, Memory and I/O Units. * Explain the pipelining principles, Data dependencies and hazards, SIMD and Multiprocessor concepts. | | | |
| **Module -1** | | | **Teaching Hours** |
| |  | | --- | | BASIC STRUCTURE OF COMPUTERS  Computer types, Functional units, Basic operational concepts, Number Representation and Arithmetic Operations, Character Representation, Problems.  **Text 1: Ch 1: 1.1, 1.2, 1.3, 1.4, 1.5, 1.9** | | | | **5 Hours** |
| **Module -2** | | | |
| |  | | --- | | INSTRUCTION SET ARCHITECTURE  Memory locations and addresses, Memory operations, Instructions and Instruction Sequencing, Addressing modes, CISC Instruction Sets, RISC and CISC Styles, Example Programs.  **Text 1: Ch 2: 2.1, 2.2, 2.3, 2.4, 2.10, 2.11, 2.12, 2.15** | | | | **5 Hours** |
| **Module – 3** | | | |
| ARITHMETIC AND LOGIC UNIT  Hardware for addition and subtraction, Multiplication, Hardware implementation, Booth’s algorithm, Division, Floating point representation, IEEE standard floating point representation, Floating point arithmetic.  **Text 2: Ch 9: 9.3, 9.4, 9.5** | | | **7 Hours** |
| **Module-4** | | | |
| CONTROL UNIT  Basic concepts, buses-bidirectional, single bus, 2 bus, 3 bus organization design methods-comparison of hardwired and micro-programmed approach, hardwired control design, Booths multiplier design, processing section design of booths multiplier, Booths multiplier controller, sequence controller design, Micro-programmed control unit: Micro-programmed control organization, Micro-programmed multiplier control unit for booths multiplier.    **Text 3: Ch 4: 4.1 to 4.3.2** | | | **10 Hours** |
| **Module-5** | | | |
| |  | | --- | | MEMORY SYSTEMS  Basic concepts, Internal organization of memory chips, Structure of Larger Memories, Memory Hierarchy, Cache memories-mapping functions, Placement strategies, Replacement algorithms, Performance considerations, Virtual memories, Magnetic hard disk  **Text 1: Ch 8: 8.1, 8.2.1, 8.2.5, 8.5, 8.6, 8.6.1, 8.7, 8.8, 8.10, 8.10.1, 8.12**  **Text 3: Ch 5: 5.8** | | | | **10 Hours** |
| **Module-6** | | | |
| INPUT/OUTPUT ORGANIZATION  Accessing I/O devices, I/O Device Interface, Program-Controlled I/O, Interrupts, Enabling and Disabling Interrupts, Handling Multiple Devices, Controlling I/O Device Behavior, Processor Control Registers, Direct Memory Access.  **Text 1: Ch 3: 3.1, 3.1.1, 3.1.2, 3.2**, **Ch 8: 8.4** | | | **3 Hours** |
| **Module-7** | | | |
| INTRODUCTION TO PARALLEL ARCHITECTURE  Pipelining- Basic Concept, Pipeline Organization, Pipelining Issues, Data Dependencies, Operand Forwarding, Handling Data Dependencies in Software, Memory Delays, Branch Delays, Unconditional Branches, Conditional Branches, The Branch Delay Slot, Hardware Multithreading,  Vector (SIMD) Processing, Graphics Processing Units (GPUs), Shared-Memory Multiprocessors, Interconnection Networks, Cache Coherence, Write-Through Protocol, Write-Back protocol, Snoopy Caches, Directory-Based Cache Coherence  **Text 1: Ch 6: 6.1 – 6.6, Ch 12: 12.1 – 12.4** | | | **8 Hours** |
| **Course outcomes:** | | | |
| After studying this course, students will be able to:   * Outline the Computer Hardware and Software, Methodology of machine instructions, addressing techniques and instruction sequencing. * Analyze the Number Systems, Positional number systems, Integer and Floating point arithmetic. * Design the control unit. * Recall about the basics of memory design of computer systems * Explain about the typical I/O techniques. * Explain the pipelining principles, Data dependencies and hazards, SIMD and Multiprocessor concepts. | | | |
| **Text Books:**   1. Carl Hamacher, ZvonkoVranesic and SafwatZaky, “Computer Organization and Embedded Systems”, Sixth edition, McGraw Hill Publication, 2012. 2. William Stallings, “Computer Organization and Architecture – Designing for Performance”, 9th edition, PHI, 2015. 3. Mohammed Rafiquzzaman and Rajan Chandra, “Modern Computer Architecture”, Galgotia Publications Pvt. Ltd., 2010. | | | |
| **Reference Books:**   1. D.A. Patterson and J.L.Hennessy, "Computer Organization and Design-The Hardware/Software Interface", Fifth Edition, Morgan Kaufmann, 2014. 2. J.P.Hayes, "Computer Architecture and Organization", McGraw Hill Publication, 1998. | | | |